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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,260	12/16/2004	Andrew Steele	GB020103	8331

24737 7590 06/28/2006

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EXAMINER	
KAPLAN, HAL IRA	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/518,260	STEELE, ANDREW	
	Examiner	Art Unit	
	Hal I. Kaplan	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 10* is/are allowed.

6)☒ Claim(s) *1,2 and 4-8* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file. The copy of the international application and English language translation of the international application referred to in Applicant's remarks have not been received.

Specification

2. The disclosure is objected to because of the following informalities: Page 9, line 3 contains the phrase "is used to". It appears this should be "is connected to".

Appropriate correction is required.

Drawings

3. The drawings were received on May 9, 2006. These drawings are accepted. In Applicant's remarks, Applicant stated that reference number 17 was added to Figure 1. There is no reference number 17 in Figure 1, and the Examiner has assumed that this was an error and should have been reference number 18.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by the US patent of Venema (4,633,168).

As to claim 1, Venema, drawn to a measuring system for determining the reactance ratio of a pair of reactive devices, teaches, in Figure 1, a signal generator for generating a pulse width modulated signal, comprising: matched reference and modulation ramp circuits, each including a current source (V_s/R_1,V_s/R_2) (see Figure 1), a capacitance (C_1,C_2) arranged to be charged by the current output from the current source (V_s/R_1,V_s/R_2) (see column 1, lines 64-66), a switch (T_1,T_2) for discharging the capacitance (C_1,C_2) (see column 2, lines 11-15 and 44-49), and a voltage detector (11,12) for detecting a predetermined charge on the capacitance (C_1,C_2) (see column 2, lines 20-23 and 51-54); wherein the output (V_T) of the voltage detector (12) of the reference ramp circuit controls the switch (T_1,T_2) of both the reference and the modulation ramp circuits (see column 2, lines 11-15, 44-49, and 54-56, and Figure 1); and the output (V_0) of the voltage detector (11) of the modulation ramp circuit is connected to an output for providing the pulse width modulated signal (see Figure 1).

As to claim 2, in each of the measurement and modulation ramp circuits of Venema, the current source (V_s/R_1,V_s/R_2) is connected to the capacitance (C_1,C_2) at a measurement node (see Figure 1); the voltage detector (11,12) has a sense input and an output (V_T,V_0) with the sense input being connected to the measurement node (see Figure 1), for detecting the voltage on the measurement node and outputting a control signal on the output (V_T,V_0) under predetermined conditions (see column 2, lines 20-23 and 51-56); the switch (T_1,T_2) is arranged across the capacitance (C_1,C_2) (see Figure 1); and the switch (T_1,T_2) has a control input (see Figure 1), the switch (T_1,T_2) being arranged to be closed by a signal on the control input for discharging the capacitance

the capacitance in response to the control signal (see column 2, lines 11-15 and 44-49); the capacitance (C_1,C_2), voltage detector (11,12) and switch (T_1,T_2) of the reference and modulation ramp circuits are matched (see column 1, 64-66; if the capacitors may take any forms, they can be matched); and the control output (V_T) of the voltage detector (12) on the reference ramp circuit is connected to the control input of the switches (T_1,T_2) of both the reference and modulation ramp circuits.

As to claim 4, in the signal generator of Venema, the switch in each ramp circuit is a transistor (T_1,T_2) having controlled terminals connected across the capacitance (C_1,C_2) and the control terminal connected to the output of the voltage detector (12) of the reference ramp circuit.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venema.

Venema discloses all of the claimed features, as set forth above, except for the modulation and reference ramp circuits being integrated on a single semiconductor substrate. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to integrate the modulation and ramp circuits on a single semiconductor substrate because it has been held that merely making integral is a matter of obvious engineering choice and not a patentable distinction. *In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) (A claim to a fluid transporting vehicle was rejected as obvious over a prior art reference which differed from the prior art in claiming a brake drum integral with a clamping means, whereas the brake disc and clamp of the prior art comprise several parts rigidly secured together as a single unit. The court affirmed the rejection holding, among other reasons, "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice."). See MPEP §2144.04(V)(B).

9. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venema in view of the US patent of Sase et al. (6,798,180).

As to claim 6, Venema discloses all of the claimed features, as set forth above, except for a switching dc-dc converter circuit. Sase, drawn to a power-supply device, teaches, in Figure 1, a switching dc-dc converter circuit comprising a dc input (Vi); a dc output (Vo); a signal generator (PWM); and a switching module (Q1,Q2) connected between the dc input (Vi) and the dc output (Vo) and containing at least one switch (Q1,Q2) controlled by the output of the signal generator to convert an input dc voltage into an output dc voltage (see column 3, lines 37-41 and 52-55). It would have been

obvious to one of ordinary skill in the art, at the time of the invention, to build the circuit of Sase with the signal generator of Venema, because the circuit of Sase requires a pulse width modulated signal generator.

As to claim 7, Sase does not disclose the power switching comprise comprising a device package, but it would have been obvious to one of ordinary skill in the art, at the time of the invention, to build the device of Sase including the signal generator (PWM) and at least one power transistor switch (Q1,Q2) in a device package because it has been held that merely making integral is a matter of obvious engineering choice and not a patentable distinction. *In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) (A claim to a fluid transporting vehicle was rejected as obvious over a prior art reference which differed from the prior art in claiming a brake drum integral with a clamping means, whereas the brake disc and clamp of the prior art comprise several parts rigidly secured together as a single unit. The court affirmed the rejection holding, among other reasons, "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice."). See MPEP §2144.04(V)(B).

As to claim 8, the device of Sase comprises first (Q1) and second (Q2) power transistors wherein the signal generator (PWM) is arranged to switch on the first power transistor (Q1) only when the second transistor (Q2) is switched off and to switch on the second transistor (Q2) only when the first transistor (Q1) is switched off (see column 3, lines 52-57).

Allowable Subject Matter

10. Claims 9 and 10 are allowed.

11. The following is an examiner's statement of reasons for allowance:

Claims 9 and 10 are allowed because none of the prior art of record teaches or discloses supplying a modulated current to charge the capacitance of the modulation ramp circuit, in combination with the remaining claimed features.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

12. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

Claim 3 contains allowable subject matter because none of the prior art of record teaches or discloses supplying a modulated current to charge the capacitance of the modulation ramp circuit, in combination with the remaining claimed features.

Response to Arguments

14. Applicant's arguments, see Remarks, filed May 9, 2006, with respect to the objections have been fully considered and are persuasive, except as set forth above.

The objections have been overcome and are respectfully withdrawn, except as set forth above.

15. Applicant's arguments filed May 9, 2006, with respect to the rejection of claim 1 under 35 U.S.C. 102(b) as being anticipated by Venema have been fully considered but they are not persuasive.

As to claim 1, Applicant contends that Venema only discloses a single current source (DC power supply 10). DC power supply 10, however, is a voltage source. The Examiner respectfully contends that "V_s/R_1" and "V_s/R_2" comprise passive voltage sources, and the claimed invention makes no distinction between active and passive voltage sources. Claims 2 and 4-8 stand rejected, as no further arguments regarding them have been presented.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal I. Kaplan whose telephone number is 571-272-8587. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

hik

ROBERT L. DEBERADINIS
PRIMARY EXAMINER